WHAT IS CLAIMED IS:

1. A method of manufacturing a microelectronics device, comprising:

providing a substrate having an active layer, a dielectric layer and a structural layer, wherein the active layer is formed over the dielectric layer and the dielectric layer is formed over the structural layer;

forming an opening through the active layer thereby exposing a surface of the dielectric layer and defining active layer sidewalls; and

forming a spacer covering a first portion of the exposed dielectric layer surface and substantially spanning one of the active layer sidewalls.

2. The method of claim 1 further comprising forming an etch stop layer over the active layer, wherein the opening is formed through the active layer and the etch stop layer thereby defining etch stop layer sidewalls substantially aligned with the active layer sidewalls, wherein the spacer substantially spans one of the active layer sidewalls and one of the etch stop layer sidewalls.

3. The method of claim 1 further comprising:

cleaning at least a second portion of the exposed dielectric layer surface.

4. The method of claim 3 wherein the cleaning includes chemical etching with an etchant chemistry comprising hydrofluoric acid.

5. The method of claim 3 wherein the cleaning includes plasma etching.

6. The method of claim 5 wherein the plasma etching includes a plasma chemistry comprising fluorine.

7. The method of claim 3 wherein the cleaning includes vapor etching.

8. The method of claim 1 further comprising forming a gate electrode over the active layer.

9. The method of claim 1 further comprising forming a silicide layer over the active layer.

10. The method of claim 1 wherein the spacer comprises silicon dioxide.

11. The method of claim 1 wherein the active layer comprises strained silicon.

12. The method of claim 1 wherein the active layer has a thickness ranging between about 100 Angstroms and about 1000 Angstroms.

13. A microelectronics device, comprising:

a substrate including a structural layer, a dielectric layer located over the structural layer, and an active layer located over the dielectric layer;

an opening extending through the active layer thereby exposing a surface of the dielectric layer and defining active layer sidewalls;

a spacer covering a first portion of the exposed dielectric layer surface and substantially spanning one of the active layer sidewalls; and

a semiconductor device located at least partially over the active layer.

14. The microelectronics device of claim 13 further comprising an etch stop layer located over the active layer, wherein the opening extends through the etch stop layer thereby defining etch stop layer sidewalls substantially aligned with the active layer sidewalls, wherein the spacer substantially spans one of the active layer sidewalls and one of the etch stop layer sidewalls.

15. The microelectronics device of claim 13 further comprising a silicide layer located over the active layer.

16. The microelectronics device of claim 13 wherein the spacer comprises silicon dioxide.

17. The microelectronics device of claim 13 wherein the active layer comprises strained silicon.

18. The microelectronics device of claim 13 wherein the active layer has a thickness ranging between about 100 Angstroms and about 1000 Angstroms.

19. The microelectronics device of claim 13 wherein the active layer comprises:

a silicon layer;

a silicon germanium layer located over the silicon layer; and

a strained silicon layer located over the silicon germanium layer.

20. A integrated circuit device, comprising:

a substrate including a structural layer, a dielectric layer located over the structural layer, and an active layer located over the dielectric layer;

a plurality of openings each extending through the active layer thereby exposing a surface of the dielectric layer and defining a plurality of active layer islands each having sidewalls;

a plurality of spacers each covering a portion of the exposed dielectric layer surface and substantially spanning one of the plurality of active layer sidewalls;

a plurality of semiconductor devices each located at least partially over a corresponding one of the plurality of active layer islands; and

at least one interconnect electrically connecting ones of the plurality of semiconductor devices.

21. The integrated circuit device of claim 20 wherein the dielectric layer comprises diamond.

22. The integrated circuit device of claim 20 wherein the active layer comprises strained silicon.

23. The integrated circuit device of claim 20 wherein the active layer comprises diamond.

24. The integrated circuit device of claim 20 wherein the active layer comprises:

a silicon layer;

a silicon germanium layer located over the silicon layer; and

a strained silicon layer located over the silicon germanium layer.